PRELIMINARY

Accel Semiconductor

AS6001 / AS6002

FM Stereo Transmitter

FEATURES

- **Highly integrated FM stereo transmitter**
- **Patent-pending architecture**
- **Low power operation, extremely suitable for portable devices**
- **Ultra low standby current in 10uA with PDN enable**
- **LDO embedded for easy power supply design**
- **3-wire digital control interface for flexible channel programming and control (AS6001)**
- **4-wire parallel control interface for easy channel programming and control (AS6002)**
- **87 – 108 MHz with 0.1MHz step PLL-based continuous tuning for China, Europe and North America (AS6001)**
- **87.7 – 88.9MHz and 106.7 – 107.9MHz with 0.2MHz step PLL-based continuous tuning (AS6002)**
- **Less off chip components**
- **Small footprint SSOP-20 and QFN-20 package**

APPLICATION

MP3 Player
Cellular Handsets
Wireless Microphone
Personal Media Player
Personal Computer
Game Machine
Car Audio

GENERAL DESCRIPTION

The AS6001/AS6002 is an innovative highly integrated FM stereo transmitter. It is the first generation of FM transmitter IC designed using Accel's patent-pending RF technology.

It consists of a stereo encoder and FM transmitter. The stereo encoder is based on signal processing to encode analog stereo audio input signal and generate a composite FM signal with MAIN, SUB and pilot signal from a 7.6MHz oscillator. The FM transmitter uses direct frequency synthesis to radiate FM wave to the air by modulating the carrier signal with the composite signal.

The AS6001/AS6002 is designed for portable application as well as general application. The 1.8V operation voltage and as low as 18mA quiescent current make it extremely suitable for portable devices such as MP3 and mobile phone. It also embeds LDO power regulator to make power supply design easy and flexible.

The AS6001 has a 3-wire digital control interface for external controller easy and flexible to program and control the transmitting channel. The transmitting channel is from 87 to 108 MHz with 0.1MHz step continuous tuning. So it is suitable for China, Europe and North America.

ORDERING INFORMATION

PART	PACKAGE-PIN
AS6001BCS	SSOP-20
AS6001BCQ	QFN-20
AS6002BCS	SSOP-20
AS6002BCQ	QFN-20

ABSOLUTE MAXIMUM RATINGS (T=25℃)

Parameter	Symbol	Limits	Unit	Conditions
supply voltage	Vddh	5	V	1
Data input voltage	V_{in-D}	-0.3~Vddh+0.3	V	2
VPLL output voltage	V_{OUT-P}	-0.3~Vddh+0.3	V	3
Power dissipation	Pd	200	mW	
Storage temperature	Tstg	-55~+125	°C	

Table 1 Absolute Maximum Ratings

1. Pin5 of AS6001BCS and AS6002BCS and Pin8 of AS6001BCQ and AS6002BCQ.
2. Pin 14, 15, 16, 17 of AS6001BCS and Pin 17, 18, 19, 20 of AS6001BCQ, Pin14, 15, 16, 17, 18 of AS6002BCS and Pin 3, 17, 18, 19, 20 of AS6002BCQ.
3. Pin 7 of AS6001BCS and AS6002BCS, Pin10 of AS6001BCQ and AS6002BCQ.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operating supply voltage	Vddh	1.8		4	V	1
Operating temperature	Topr	-40	-	+85	°C	
Audio input level	Vin_A	-	-	-20	dBV	2
Audio input frequency band	Fin_A	20	-	15K	Hz	2
Transmission frequency	Frx	87M	-	108M	Hz	3
Control terminal "H" level input voltage	V_{IH}	0.8Vddh	-	Vddh	V	4
Control terminal "L" level input voltage	V_{IL}	GND	-	0.2Vddh	V	4

Table 2 Recommended operating conditions

1. Pin5 of AS6001BCS and AS6002BCS and Pin8 of AS6001BCQ and AS6002BCQ.
2. Pin2, 19 of AS6001BCS and AS6002BCS, Pin1, 5 of AS6001BCQ and AS6002BCQ.
3. Pin9 of AS6001BCS and AS6002BCS, Pin11 of AS6001BCQ and AS6002BCQ.
4. Pin 14, 15, 16, 17 of AS6001BCS and Pin 17, 18, 19, 20 of AS6001BCQ, Pin14, 15, 16, 17, 18 of AS6002BCS and Pin 3, 17, 18, 19, 20 of AS6002BCQ.

FUNCTION BLOCK DIAGRAM & PIN ASSIGNMENT

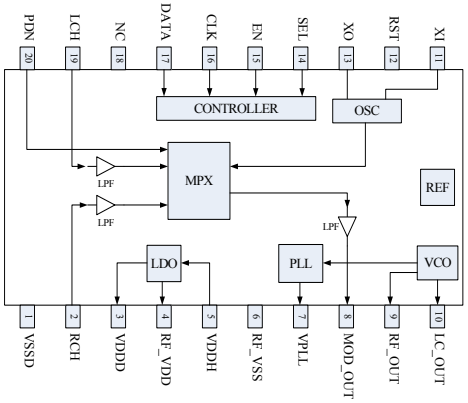


Figure 1 AS6001 Block Diagram and Pin Assignment of SSOP-20

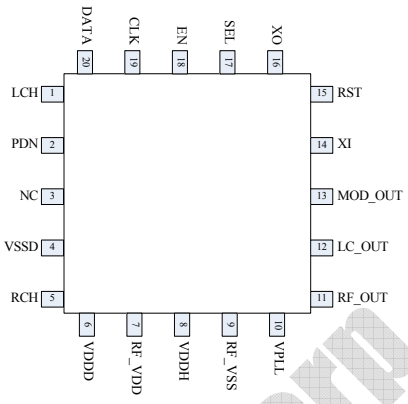


Figure 2 AS6001 Pin Assignment of QFN-20

PIN DESCRIPTION

SSOP-20 PIN Number	QFN PIN Number	PIN Name	I/O	PIN Description
1	4	VSSD	P	Power ground for IC
2	5	RCH	I	Right channel input
3	6	VDDD	P	Power supply for digital
4	7	RF_VDD	P	Power supply for RF
5	8	VDDH	P	Power supply for IC
6	9	RF_VSS	G	Power ground for RF
7	10	VPLL	O	PLL charge pump output
8	13	MOD_OUT	I/O	Modulation signal output
9	11	RF_OUT	O	RF signal output
10	12	LC_OUT	O	VCO off chip tank connection
11	14	XI	I	Crystal in
12	15	RST	I	Reset input signal
13	16	XO	I	Crystal out
14	17	SEL	I	Pre-emphasis time constant selection signal
15	18	EN	I	3-wire enable input
16	19	CLK	I	3-wire clock input
17	20	DATA	I	3-wire data input
18	3	NC	N	No connect
19	1	LCH	I	Left channel input
20	2	PDN	I	IC power down

Table 3 AS6001 Pin description of SSOP-20 and QFN-20

FUNCTION BLOCK DIAGRAM & PIN ASSIGNMENT

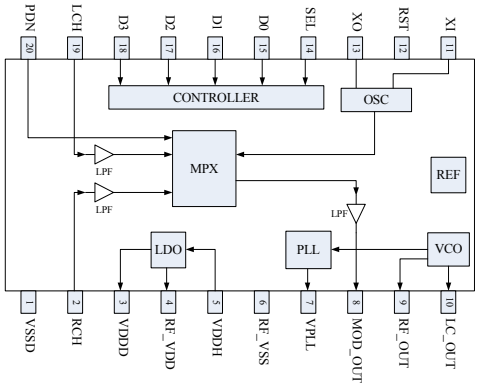


Figure 3 AS6002 Block Diagram and Pin Assignment of SSOP-20

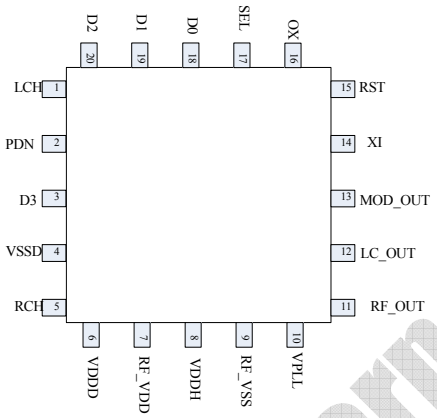


Figure 4 AS6002 Pin Assignment of QFN-20

PIN DESCRIPTION

SSOP-20 PIN Number	QFN PIN Number	PIN Name	I/O	PIN Description
1	4	VSSD	P	Power ground for IC
2	5	RCH	I	Right channel input
3	6	VDDD	P	Power supply for digital
4	7	RF_VDD	P	Power supply for RF
5	8	VDDH	P	Power supply for IC
6	9	RF_VSS	G	Power ground for RF
7	10	VPLL	O	PLL charge pump output
8	13	MOD_OUT	I/O	Modulation signal output
9	11	RF_OUT	O	RF signal output
10	12	LC_OUT	O	VCO off chip tank connection
11	14	XI	I	Crystal in
12	15	RST	I	Reset input signal
13	16	XO	I	Crystal out
14	17	SEL	I	Pre-emphasis time constant selection signal
15	18	D0	I	PLL frequency selection input
16	19	D1	I	PLL frequency selection input
17	20	D2	I	PLL frequency selection input
18	3	D3	I	PLL frequency selection input
19	1	LCH	I	Left channel input
20	2	PDN	I	IC power down

Table 4 AS6002 Pin description of SSOP-20 and QFN-20

ELECTRICAL CHARACTERISTIC (T=25 ^{O}C VDDH=2.7V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current	I_Q	14	16	20	mA	
Standby current	I_{Stby}	-	10		uA	PDN="1"
Total harmonic distortion	THD	-	0.1	0.3	%	Vin=-20dBV L+R Freq=400Hz
Channel balance	C.B	-0.5	0	+0.5	dB	Vin=-20dBV L+R Freq=400Hz
Channel separation	Sep	30	40		dB	Vin=-20dBV L+R Freq=400Hz
Input voltage amplitude limit			-20		dBV	LCH and RCH
Input output gain	Gv	-2	0	+2	dB	Vin=-20dBV L+R Freq=400Hz
Pilot modulation rate	Mp	12	15	18	%	Vin=-20dBV L+R, Freq=400Hz
Sub carrier rejection ratio	SCR	-	-40	-30	dB	Vin=-20dBV L+R Freq=400Hz
Pre-emphasis time constant	T_{pre}		50/ 75		us	Vin=-20dBV L+R Freq=400Hz
LPF cut off frequency	$f_{c(LPF)}$		20K		Hz	LCH and RCH
Transmission output level	Vtx	106	108	110	dBuV	Frx=108MHz RF_OUT, 75Ω loading
"H" level input current	I_{IH}	-	-	1	uA	
"L" level input current	I_{IL}	-1	-	-	uA	
Positive power supply	Vddd	1.6	1.8	2.0	V	On chip regulated
Positive RF power supply	Vdd_RF	1.6	1.8	2.0	V	On chip regulated

Table 5 Electrical characteristic

OPREATION

3-wire Interface (AS6001)

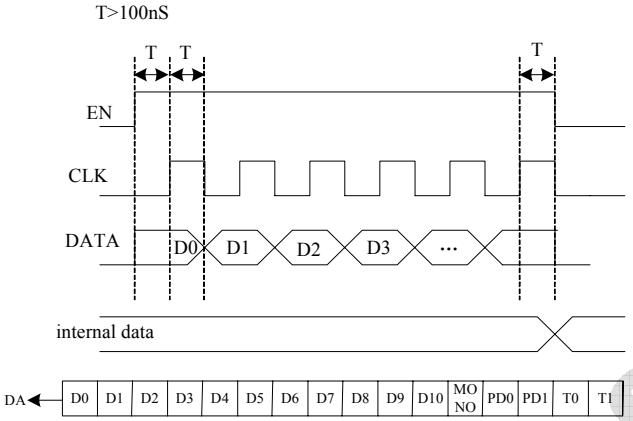


Figure 5 3-wire Interface Timing Diagram

No.	Control unit/Data	Contents
(1)	PROGRAM COUNTER D0~D10	It is the data which sets the program counter number of dividing. This data can set a transmission frequency. It's a binary value. It sets D10 with MSB and D0 with LSB Example: In case of 99.7MHz oscillation 99.7MHz/100KHz(freq)=997→3E5(HEX) Valid values are between 366(HEX) to 438(HEX) 1 0 1 0 0 1 1 1 1 1 0 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 LSB MSB
(2)	MONO	It changes stereo and mono operation 1: stereo operation 0: mono operation (L+R)
(3)	PD0,PD1	It controls the charge pump output voltage PD0 | PD1 | charge pump output 0 | 0 | usual operation 0 | 1 | force low 1 | 0 | force high 1 | 1 | high impedance
(4)	T0,T1	T0 and T1 are for test always set T0 "1" always set T1 "0"

Table 6 Explanation of Serial Data*

*Notes: There is no default value of serial data.

4-wire Parallel Interface (AS6002)

control data				Frequency
D0	D1	D2	D3	
L	L	L	L	87.7MHz
H	L	L	L	87.9MHz
L	H	L	L	88.1MHz
H	H	L	L	88.3MHz
L	L	H	L	88.5MHz
H	L	H	L	88.7MHz
L	H	H	L	88.9MHz
H	H	H	L	PLL stops. VPLL terminal supports high impedance
L	L	L	H	106.7MHz
H	L	L	H	106.9MHz
L	H	L	H	107.1MHz
H	H	L	H	107.3MHz
L	L	H	H	107.5MHz
H	L	H	H	107.7MHz
L	H	H	H	107.9MHz
H	H	H	H	PLL stops. VPLL terminal supports high impedance

Table 7 Explanation of Parallel Data

SEL Pin

The SEL pin is pre-emphasis time constant selection.
L: 50uS
H: 75uS

RST Pin

The RST pin is IC reset input.
L: reset disable
H: reset enable

PDN Pin

The PDN pin controls the IC power on or off.
L: power on
H: power off

APPLICATION CIRCUITS

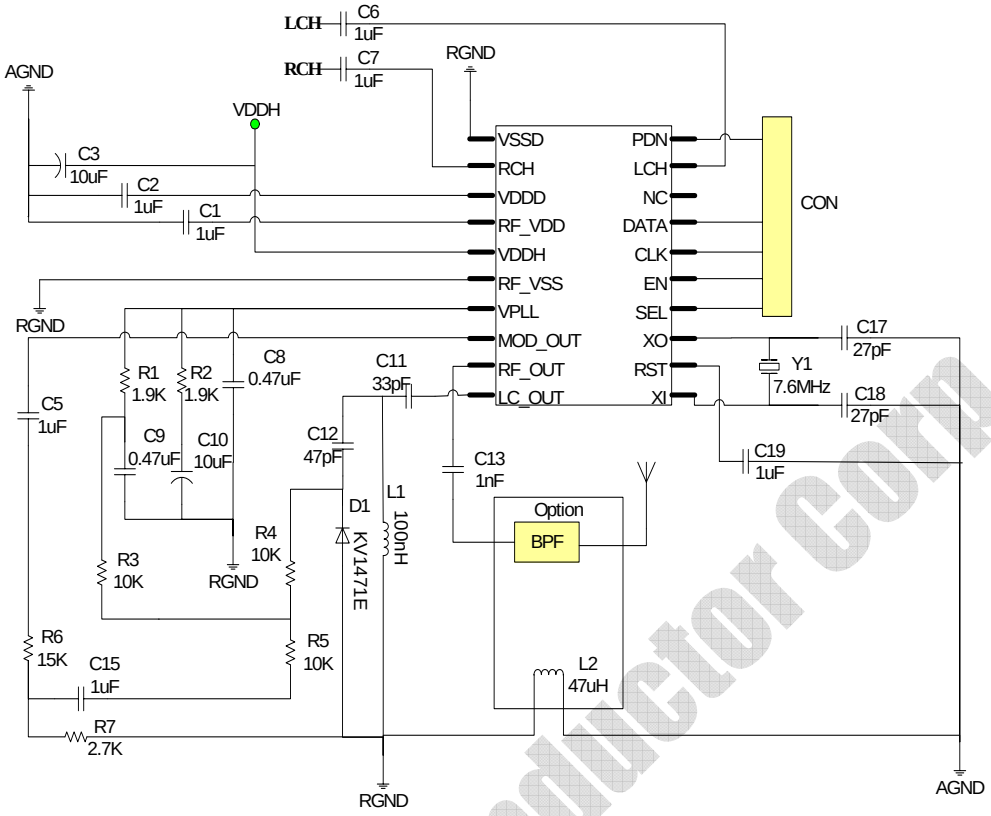


Figure 6 AS6001 Application Circuit

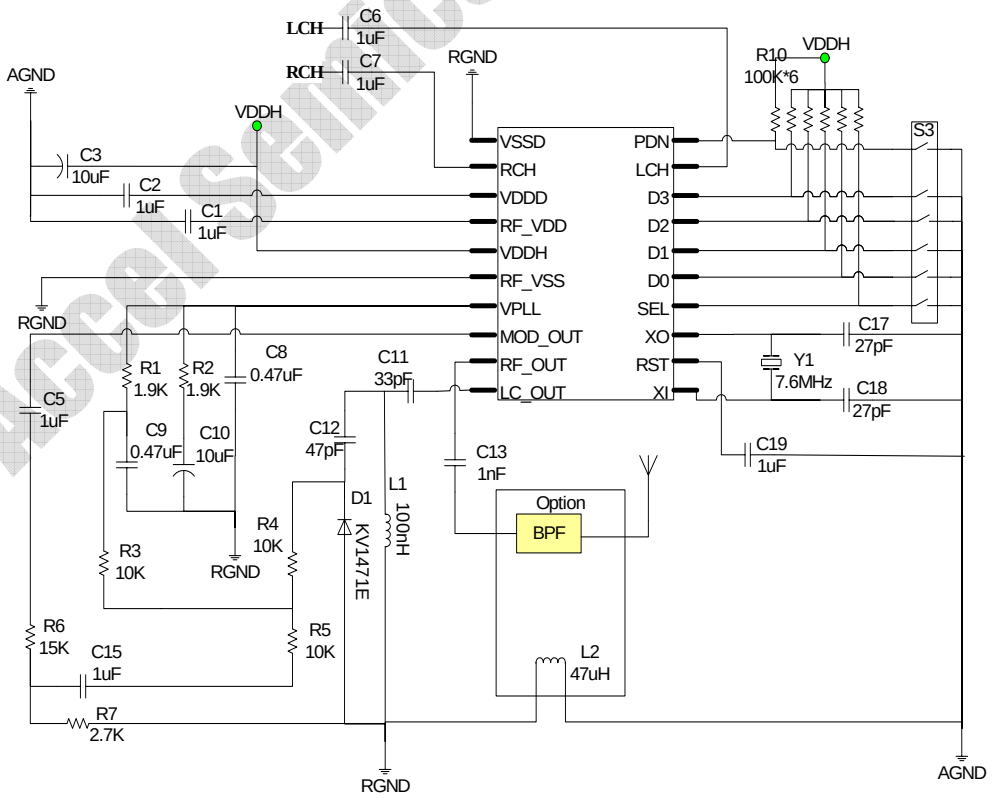
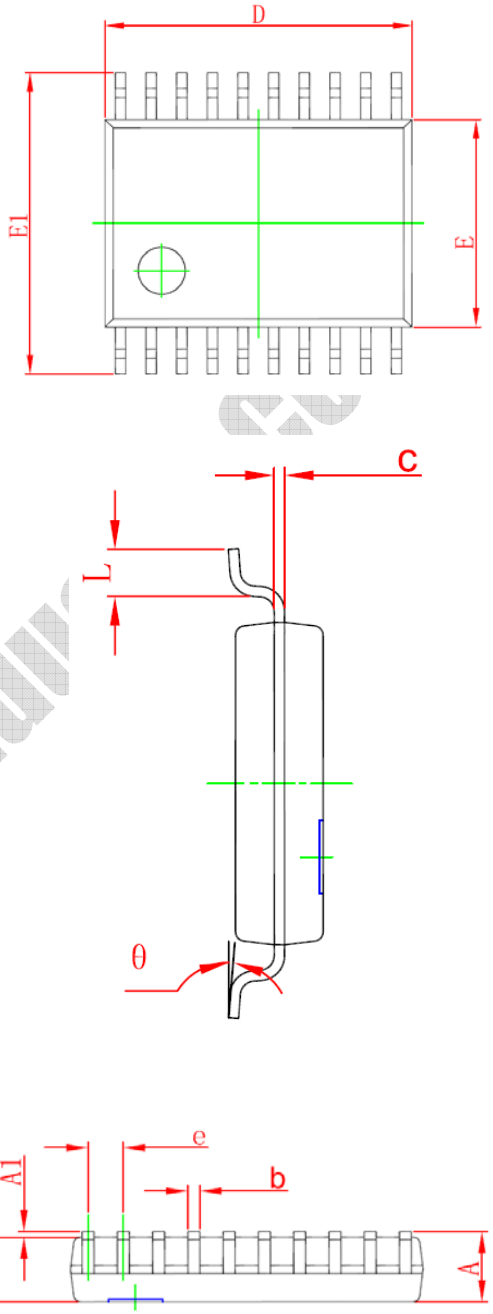


Figure 7 AS6002 Application Circuit

PACKAGE DIMENSIONS

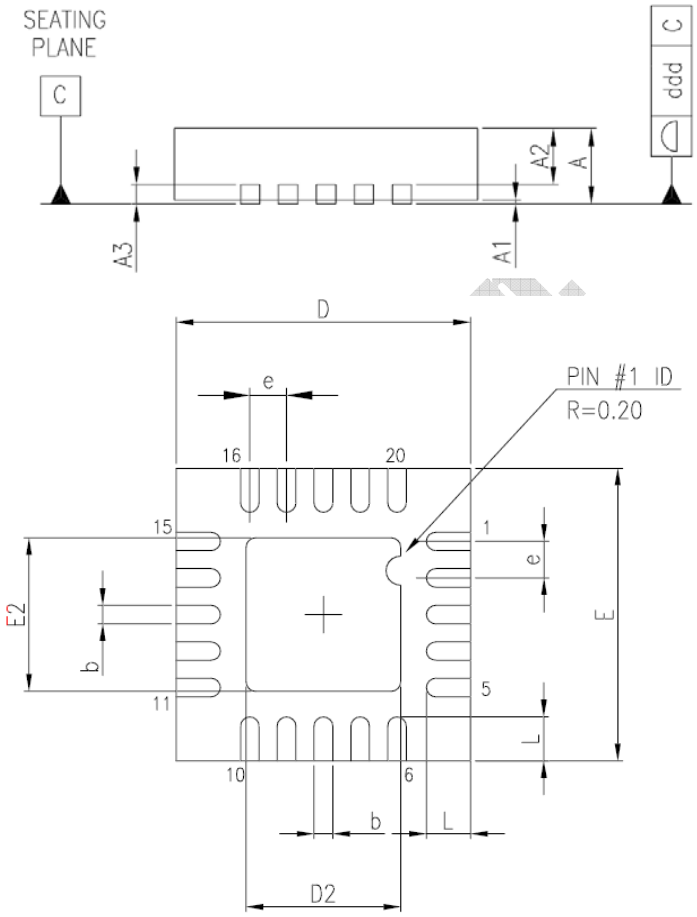
SSOP-20

DIM.	Millmeter		
	MIN.	TYP	MAX.
A	-	-	1.450
A1	0.050	-	0.200
A2	1.150	-	1.250
b	0.200	-	0.310
c	0.090	-	0.200
D	6.300	-	6.700
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.65BSC		
L	0.450	-	0.750
θ	0°	-	8°



QFN20 (4x4mm)

DIM.	mm.		
	MIN.	TYP	MAX.
A	0.8	0.9	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D	3.875	4.00	4.125
D2	0.75	1.7	2.25
E	3.875	4.00	4.125
E2	0.75	1.7	2.25
e	0.45	0.50	0.55
L	0.35	0.55	0.75
ddd			0.08



CONTACT INFORMATION

Accel Semiconductor Corp.

1F, Main Building, 149 Chun Xiao Road
Shanghai, P.R. China
Tel: +86 (21) 5027 0501
Fax: +86 (21) 5027 3116
Zip: 201203
e-mail: sales@accelsemi.com
Internet: http://www.accelsemi.com

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